DESIGN OF A LOW NOISE AMPLIFIER

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Abstract:

Low Noise Amplifiers (LNAs) are critical components in radio- frequency (RF) front-end systems, responsible for amplifying extremely weak signals received from antennas while maintaining minimal noise degradation. The performance of an LNA directly impacts the sensitivity and reliability of communication systems such as wireless networks, satellite communication, and radar systems. This paper presents the design and analysis of a CMOS-based LNA using cascode topology combined with inductive source degeneration. The proposed design aims to achieve high gain, low noise figure, proper impedance matching, and improved linearity. The implementation is carried out using 90 nm CMOS technology in Cadence Virtuoso environment. Simulation results demonstrate that the proposed design achieves significant improvement in gain and noise performance while maintaining stability and low power consumption.

Index Terms -- Low Noise Amplifier, CMOS, Cascode Topology, Inductive Source Degeneration, Noise Figure, RF Front-End.

I. INTRODUCTION

A Low Noise Amplifier (LNA)is a key component in communication and sensor systems that amplifies weak input signals while introducing minimal noise, thereby preserving signal integrity and improving system sensitivity. Placed at the front end of the receiver, it is designed to achieve low noise figure (NF), high gain, good linearity, and proper impedance matching (typically 50Ω) to ensure efficient signal amplification with minimal distortion and maximum power transfer. LNAs are commonly implemented using CMOS-based MOSFETs due to their low noise and high integration capability, and employ techniques such as cascode topology and inductive source degeneration to optimize performance trade-offs between gain, noise, and bandwidth. Owing to these features, LNAs are widely used in RF and microwave applications including wireless communication, radar, satellite systems, and medical imaging.

II. LITERATURE SURVEY

Low Noise Amplifiers (LNAs) are critical in RF receiver front-end circuits, where their primary role is to amplify weak signals with minimal noise, directly impacting overall system sensitivity. Early designs focused mainly on achieving high gain but suffered from high noise figure and poor impedance matching. Later research emphasized noise reduction and efficient input matching; with studies such as Razavi (2012) highlighting the effectiveness of CMOS LNAs, and Lee and Hajimiri (2004) demonstrates inductive source degeneration for simultaneous noise optimization and impedance matching. The common-source LNA with inductive degeneration, introduced by Shaeffer and Lee (1997), achieved low noise and proper 50-Ω matching but faced limitations in gain and isolation at high frequencies. To overcome these issues, cascode architectures were developed, with ThomasH.Lee(2004) and Andreani and Mattisson (2005) showing improved gain, stability, and reduced Miller effect. Recent works, including Karanicolas (2021), Kim et al. (2023), Huang et al. (2024), and Kang et al. (2025), further enhanced CMOS LNA designs by improving gain, reducing noise figure, and optimizing performance for modern and millimeter-wave communication systems. Overall, the cascode LNA with inductive source degeneration provides an effective balance between gain, noise, impedance matching, and stability, making it a widely adopted architecture in RF applications.

III. PROPOSEDSYSTEM

The schematic design of a low noise amplifier (LNA) using Cadence Virtuoso in 90nm CMOS technology typically involves using a combination of transistor topologies to optimize gain, noise figure, and power consumption. In such a design, the common approach is to use a cascode configuration or a combination of common-gate and common-source transistor stages to achieve low noise and high gain. The input stage often uses inductive source degeneration to improve noise performance and input matching, essential for RF applications. The design process starts with selecting transistor dimensions (width and length) suitable for 90nm CMOS to balance gain and noise. The LNA schematic includes biased MOSFET transistors with carefully chosen passive components such as inductors and capacitors for impedance matching and stability.

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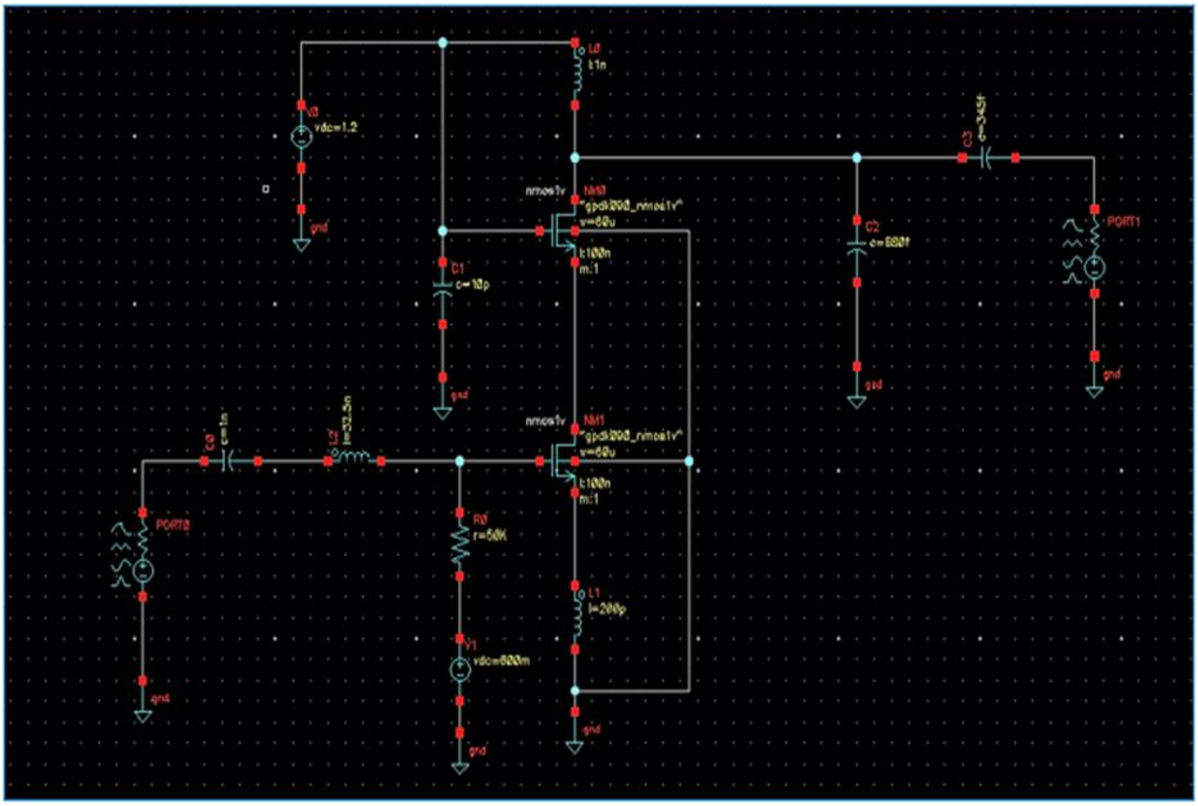

FIG : Circuit Diagram of Low Noise Amplifier

Simulation in Cadence Virtuoso involves transient, AC, and noise analysis to evaluate parameters like gain, noise figure, and input/output reflection coefficients. This approach allows achieving a gain higher than 10dBwithanoisefigureaslowas1.66 to 3 dB, depending on optimization, while consuming minimal power, often less than a few milli watts. Design iteration includes layout considerations to minimize parasitic and ensure performance at target frequencies (typicallyaround1to2.5GHzorhigher for modern wireless applications).

IV. RESULTS

A low noise amplifier (LNA) is designed to amplify very weak input signals while introducing minimal additional noise, there by preserving the signal-to-noise ratio (SNR) and improving overall receiver sensitivity. This is typically achieved using low-noise active devices such as JFETs or HEMTs,

Parameters	Target	Measured/ Simulated
Gain (s21)	10 dB to 25 dB	15 dB
Noise Figure (NF)	0.5 dB to 2 dB	0.56 dB
Input Matching (s11)	<-10 dB	-18 dB
Impedance(Zm)	50 Ohms	54 Ohms

which operate under optimized conditions

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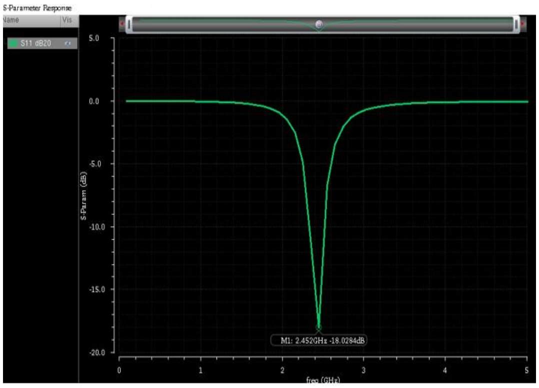

Fig. S Parameter

to suppress internal noise and enhance

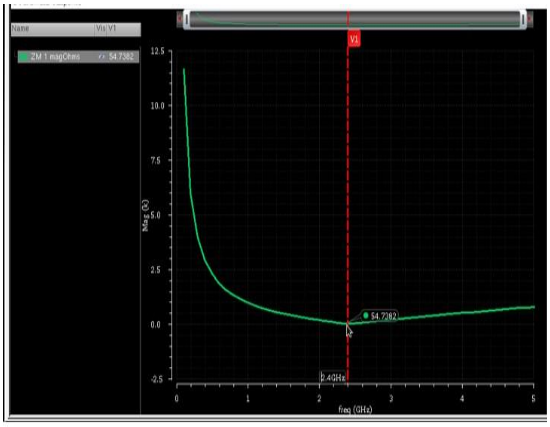

Fig. Impedance

signal quality.

The performance of the LNA is characterized by key parameters such as gain, noise figure, and linearity. The amplifier provides again in the range of 10–30dB, ensuring that weak signals are sufficiently boosted for further processing. A low noise figure, generally below 1.5 dB, indicates effective noise suppression. Linearity metrics such as input third-order intercept point (IIP3) and 1 dB compression point (P1dB) demonstrate the amplifier's ability to handle stronger signals without distortion, maintaining signal integrity.

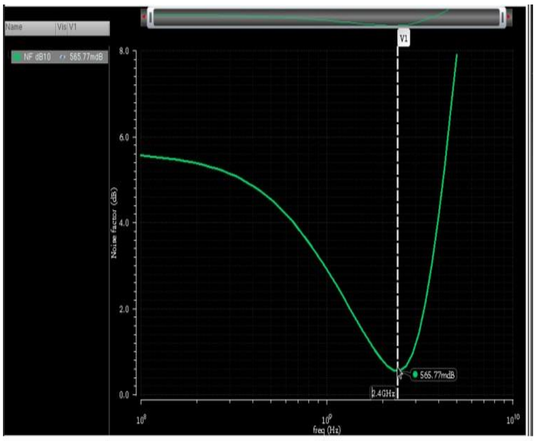

Fig. Noise Figure

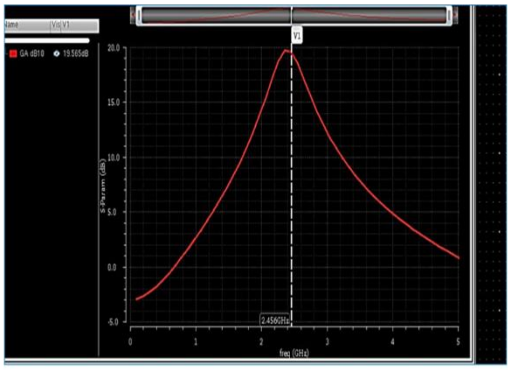

Fig. Gain

Additionally, proper impedance matching is reflected by input and output return losses around −10 dB or better, minimizing signal reflections. Internal noise sources, including voltage and current noise, also influence overall performance, particularly at low frequencies. The LNA can typically withstand maximum RF input levels of about 18–20 dBm without significant degradation.

V. CONCLUSION

The design and simulation of the Low Noise Amplifier (LNA) using Cadence Virtuoso in 90 nm CMOS technology were successfully completed, achieving high gain, low noise figure, and effective impedance matching for RF front-end applications. The use of inductive source degeneration enabled proper input matching and improved stability, while the cascode topology enhanced gain and reduced the Miller effect. Simulation results, including DC, transient, S-parameters, and noise analysis, confirmed good input-output matching, high gain, excellent isolation, and low noise performance. Overall, the proposed LNA demonstrates reliable performance, low power consumption, and suitability for modern wireless communication and RF systems.

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