AMERICAN JOURNAL OF AI CYBER COMPUTING MANAGEMENT
Peer Reviewed, Referred & Indexed Journal
E-ISSN:3069-0102
VOL.6, NO. 2(2026)

A DESIGN AND SIMULATION OF LOW POWER 18T HYBRID MASTER-SLAVE FLIP-FLOP USING FREQUENCY DIVIDER

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ABSTRACT

Frequency dividers play a crucial role in modern VLSI systems for clock generation, timing control, and communication applications. The performance of these systems highly depends on the efficiency of the flip-flop used. This paper presents the design and simulation of a low-power 18-transistor (18T) hybrid master–slave flip-flop for frequency divider applications. The proposed design combines pass-transistor logic and static CMOS logic with single-phase clocking to achieve reduced power consumption, propagation delay, and silicon area. It incorporates a level-restoring circuit in the master stage and a transistor stacking technique in the slave stage to minimize leakage power and enhance stability. Implemented using 90 nm CMOS technology, the proposed flip-flop demonstrates improved energy efficiency and reliable operation up to 1 GHz. The proposed circuit significantly reduces power dissipation and delay, making it suitable for high-speed and low- power VLSI applications.

I. INTRODUCTION

In modern Very Large-Scale Integration (VLSI) systems, power consumption, speed, and area are the key factors that determine overall circuit performance. Flip-flops are fundamental building blocks in sequential circuits and are widely used in applications such as registers, counters and frequency dividers. Among these, frequency divider circuits play a vital role in clock generation, timing control, and communication systems by reducing and stabilizing clock signals.

Conventional flip-flop designs, such as the D flip-flop, suffer from high power consumption, larger propagation delay, and increased transistor count, which limit their efficiency in high-speed and low-power applications. To overcome these challenges, optimized flip-flop architectures are required that can operate efficiently under advanced technology nodes.

This paper presents the design and simulation of a low-power 18-transistor (18T) hybrid master–slave flip-flop for frequency divider applications. The proposed design combines the advantages of pass-transistor logic and static CMOS logic, along with single-phase clocking, to achieve improved performance. A level-restoring circuit is used in the master stage to maintain signal integrity, while the slave stage employs transistor stacking to reduce leakage current.

The proposed flip-flop is implemented using 90 nm CMOS technology and evaluated in terms of power consumption, propagation delay, and energy efficiency. The results demonstrate that the proposed design outperforms conventional flip-flop architectures, making it suitable for high-speed and low- power VLSI systems.

II. LITERATURE

Low-power flip-flops are essential components in VLSI systems, widely used in registers, counters, and frequency dividers. Conventional flip-flop designs suffer from high power consumption, large transistor count, and increased delay due to high switching activity. To address these issues, several hybrid flip-flop architectures have been proposed.

Recent studies introduced 18-transistor (18T) hybrid flip-flops using true single-phase clocking (TSPC), achieving significant power reduction and improved energy efficiency by minimizing clock load and transistor usage. Further enhancements were made using master–slave configurations, where level-restoring techniques and transistor stacking are employed to reduce leakage power and improve stability.

Additionally, optimized 18T designs implemented in advanced CMOS technologies have demonstrated reduced power consumption and lower clock-to-output delay. In parallel, frequency divider circuits, which rely on flip-flops, have been improved using efficient architectures such as prescalar sand hybrid designs to achieve better performance.

Overall, existing research shows that combining 18T hybrid master–slave flip-flops with efficient frequency divider structures provides an effective solution for low-power, high-speed VLSI applications.

III. PROPOSEDMETHOD

AProposed Flip-Flop Circuit (PFC) is designed with 18 transistors. Here we use pass Transistor Logic (PTL). It is a design technique in digital circuits where transistors are used as switches to pass logic levels directly between nodes, instead of using traditional pull-up and pull-down networks as in CMOS logic. In PTL, mainly NMOS or PMOS transistors are used to transfer input signals to the output, which helps in reducing the total number of transistors required for circuit implementation.

The main advantage of PTL is its ability to achieve **low power consumption, reduced circuit complexity, and faster operation**. Since fewer transistors are used, the overall switching activity and parasitic capacitance are minimized, leading to lower dynamic power dissipation. Additionally, PTL allows faster signal propagation because the logic is transferred directly through transistors without passing through multiple stages.

However, PTL also has a limitation known as **threshold voltage drop**, where the output voltage may not reach full logic levels (especially in NMOS pass transistors passing logic '1'). To overcome this issue, **level restoring circuits** are used in the proposed design. These circuits ensure that the output signal maintains full voltage levels and improves the reliability of the flip-flop operation.

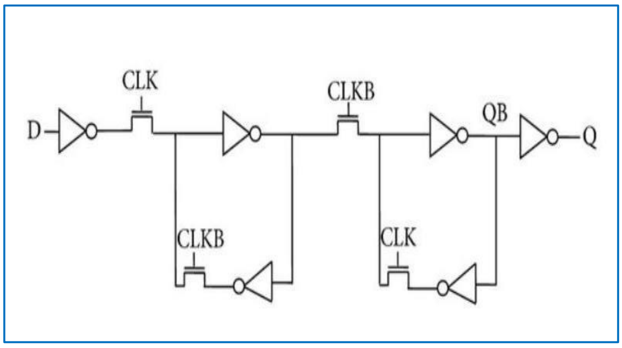

Fig3.1. Proposed Flip-Flop Circuit (PFC).

DESIGNOFF/4USINGPROPOSED FLIP-FLOP CIRCUIT (PFC)

A frequency divider is a fundamental building block in digital and mixed-signal electronic systems. It is used to generate a lower-frequency clock signal from a higher-frequency input clock. Among various divider configurations, the divide-by-4 circuit is one of the most commonly used structures due to its simplicity and wide applicability. In high-frequency systems such as phase-locked loops (PLLs), radio frequency (RF) transceivers, microprocessors, and high-speed communication systems, divide-by-4 circuits play a crucial role in clock generation and synchronization.

A high-frequency divide-by-4 circuit reduces the frequency of the input clock signal by a factor of four while maintaining signal integrity, low jitter, and minimal powerconsume.The content is structured to meet academic documentation standards and is suitable for undergraduate and postgraduate studies in VLSI and digital system design.

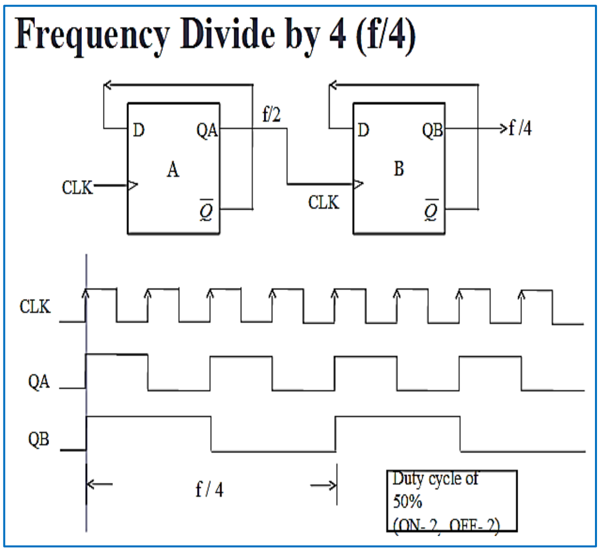

Fig3.2.Frequency Divider Circuit

Received: 05-03-2026 | Accepted: 13-04-2026 | Published: 20-04-2026 | www.ajaccm.com

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IV. RESULT

MASTER SLAVE 18T PFC

The proposed 18T master–slave PFC is designed using Cadence Virtuoso with 90 nm CMOS technology. A new library is created and linked to the 90 nm technology file.Theschematic is developed by placing NMOS and PMOS transistors, connecting them as per the circuit design, and assigning appropriate W/L ratios. Power (VDD) and ground (GND) are added, and inputs/outputs are properly labelled. After verifying the schematic using Check and Save, a symbol is generated for simulation. The circuit is simulated in ADE using transient analysis to observe output wave.

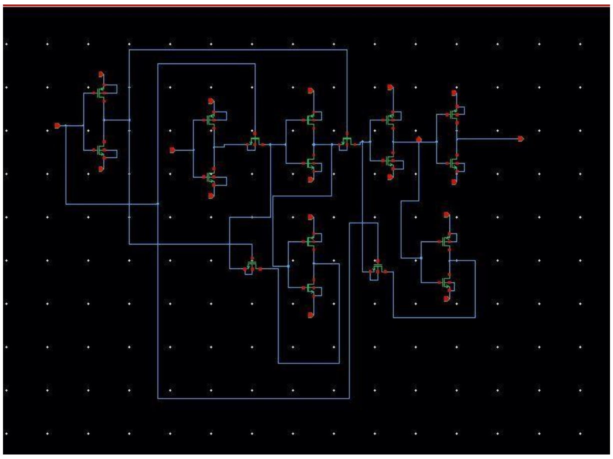

Fig4.1: Proposed Frequency Circuit

Test bench of PFC

The testbench of the proposed PFC is designed in Cadence Virtuoso using 90 nm CMOS technology. A new library is created and linked to the 90 nm PDK, and the schematic is developed by placing NMOS and PMOS transistors with L = 90 nm and suitable W values. Power supply (VDD = 1.8 V) and ground are added, and input/output nodes are properly labeled. A DC source is used for VDD, while pulse signals are applied to Data and Clock inputs. The circuit is simulated in the Analog Design Environment (ADE) using transient analysis to observe output responses (Q and Qb) and verify correct circuit operation before proceeding to layout design.

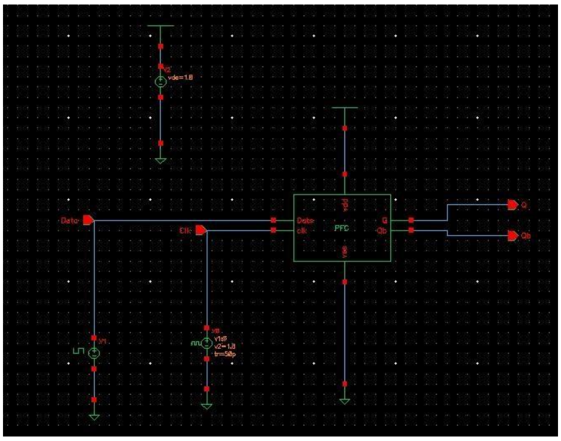

Fig4.2: Test Bench of PFC

Simulation Output of PFC

The shown wave form is the simulation output of the PFC circuit. The top signals represent the inputs, where Data (D) changes slowly and the Clock (Clk) is aperiodic square wave. The clock keeps switching between high andlowat regular intervals, while the data input changes at specific times. The circuit mainly responds to the clock signal, meaning it checks thevalueofDataonlyatparticularclockedges.

Received: 05-03-2026 | Accepted: 13-04-2026 | Published: 20-04-2026 | www.ajaccm.com

The lower signal the outputs Q and Qb (complement of Q). When the clock edge occurs, the output Q follows the value of Data, and Qb becomes the opposite of Q. For example, when Data is high during a clock edge, Q goes high and Qb goes low; when Data is low, Q becomes low and Qb becomes high. Between clock edges, the output remains constant, showing that the circuit stores the value. This confirms the proper working of the PFC as a clock-controlled storage element.

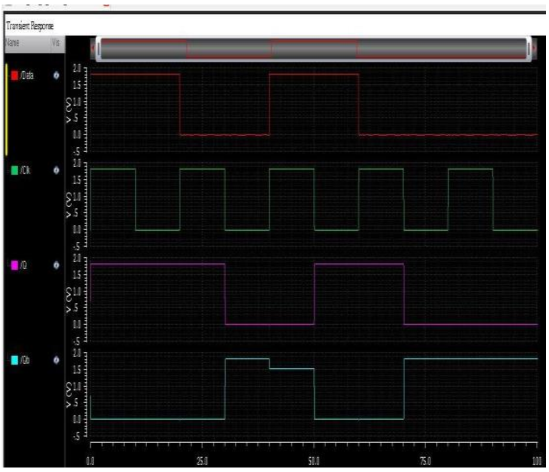

Fig6.3: Simulation Output

Frequency Divider Divider–Design and Operation

The circuit is a frequency divider implemented using two cascaded 18T hybrid master–slave flip-flops (PFCs). Bothflip-flopsaredrivenbythesameclock signal, where the output of the first stage is connected to the input of the second stage. Each flip-flop uses a hybrid logic design combining pass transistor and CMOS logic for low power and high speed.

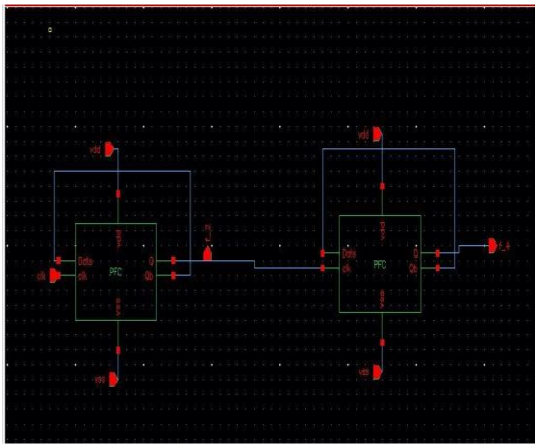

Fig6.4: Frequency Divider circuit

In operation, the first flip-flop divides the input clock frequency by 2(f/2). This output is fed to the second flip-flop, which further divides it by 2, resulting n an overall frequency division of f/4. During clock-low, the master stage captures data, and during clock-high, the slave stage transfers data to the output, ensuring synchronized operation. The design achieves reduced power consumption, lower delay, and improved performance.

Test Bench of the Frequency Divider Circuit:

This circuit is test bench of the frequency divider it’s got the final output. Here we use input is clock and the output is half of the input frequency. Weare taking two flipflops that’s why it produces two outputs. First f/2and f/4 are outputs.

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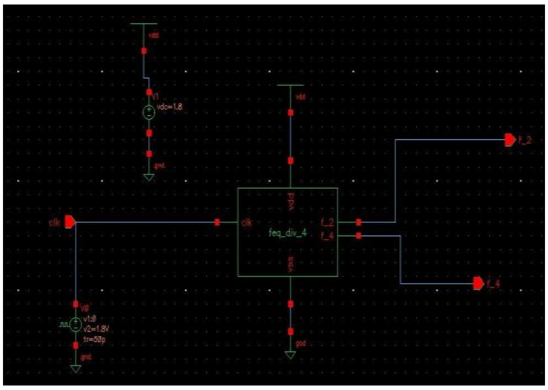

Fig6.5: Test Bench of Frequency Divider

Simulation Output of Frequency divider:

The timing diagram of a divide-by-4 circuit illustrates the relationship between the input clock and the outputs of the two flip-flops. The input clock has the highest frequency. The output of the first flip-flop toggles every alternate clock edge, and the output to the second flip-flop toggle sever alternate edge of the first flip-flop output.

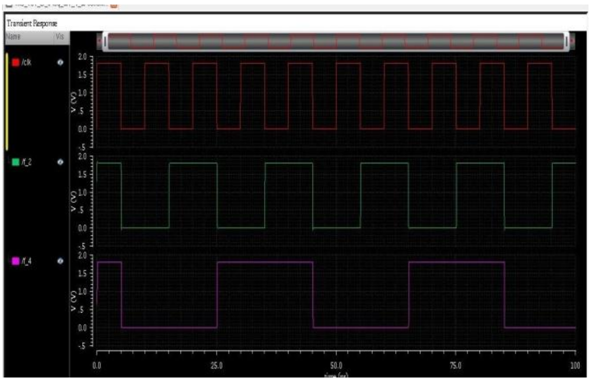

Fig 6.6: Simulation Result of Frequency

This cascading effect results in evenly spaced transitions and a stable divided clock signal. Proper timing alignment is essential to ensure correct operation, especially at high frequencies.

6.6 Size of the proposed frequency circuit:

- This image shows to size of the PFC circuit.
- The total number of nodes in the circuit is 12.
- The design uses 18T transistors, confirming the 18T flip-flop architecture.
- The circuit includes 3 voltage sources used for power supply, clock signal, and input data.

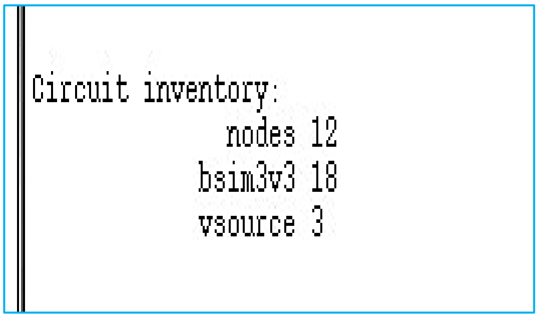

Fig6.7: Size of the proposed frequency circuit Divider

6.7 Power of proposed Frequency Circuit:

- The circuit was simulated using Cadence Virtuoso simulation tool.
- Due to continuous switching of transistors and inefficient clocking, that's why consume more power.
- To overcome this continuous switching of transistors consumes low power.
- The average current value obtained from the simulation is26.155 microwatt.
- The results confirm the low-power operation of the 18T Hybrid Master-SlaveFlip-Flop.

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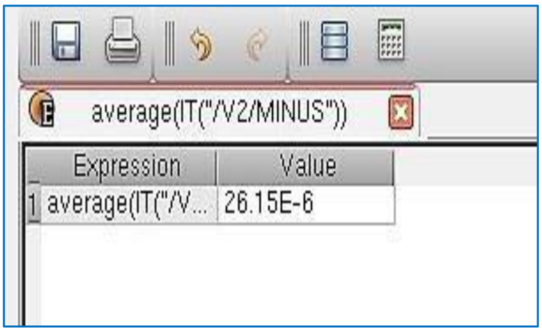

Fig6.8: Power of proposed Frequency Circuit

V. Conclusion

This paper presented the design and simulation of a low-power 18T hybrid master–slave flip-flop for frequency divider applications using 90 nm CMOS technology. The proposed design, based on hybrid logic and single-phase clocking, effectively reduces power consumption, propagation delay, and transistor count compared to conventional flip-flop architectures. By incorporating level-restoring and transistor stacking techniques, the circuit achieves improved energy efficiency andreducedleakagepower.The frequency divider implementation using cascaded flip-flops successfully demonstrates accurate frequency division with reliable operation up to high frequencies. Overall, the proposed design offers a compact, power-efficient, and high-speed solution, making It well suited for modern VLSI and communication system applications.

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